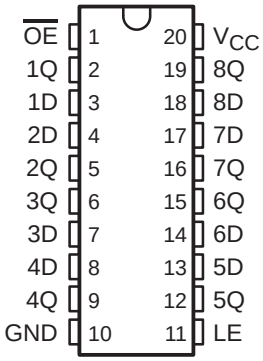
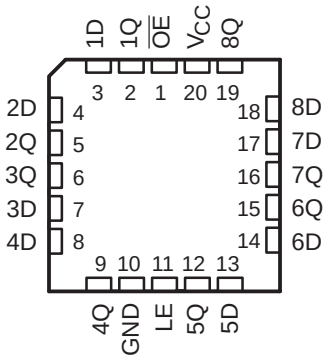
- **Inputs Are TTL-Voltage Compatible**
- **Eight High-Current Latches in a Single Package**
- **High-Current 3-State True Outputs Can Drive up to 15 LSTTL Loads**
- **Full Parallel Access for Loading**
- **Package Options Include Plastic Small-Outline (DW) and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

**SN54HCT373 . . . J OR W PACKAGE**
**SN74HCT373 . . . DW OR N PACKAGE**
**(TOP VIEW)**




**SN54HCT373 . . . FK PACKAGE**
**(TOP VIEW)**




## description

These 8-bit latches feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches of the ’HCT373 are transparent D-type latches. While the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the levels that were set up at the D inputs.

An output-enable ($\overline{OE}$) input places the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

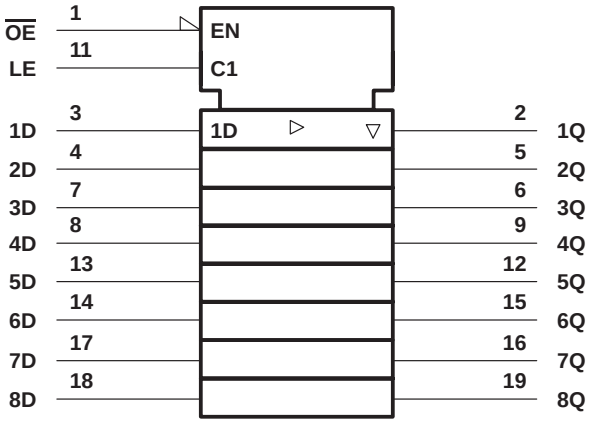
$\overline{OE}$ does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are off.

The SN54HCT373 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74HCT373 is characterized for operation from –40°C to 85°C.

**FUNCTION TABLE**
**(each latch)**

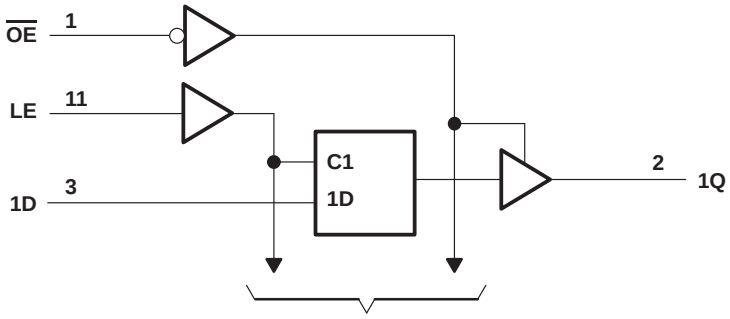
| INPUTS | | | OUTPUT |
|---|---|---|---|
| $\overline{OE}$ | LE | D | Q |
| L | H | H | H |
| L | H | L | L |
| L | L | X | $Q_0$ |
| H | X | X | Z |

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)



## absolute maximum ratings over operating free-air temperature range†

Supply voltage range, $V_{CC}$ . . . . . –0.5 V to 7 V
Input clamp current, $I_{IK}$ ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) . . . . . ±20 mA
Output clamp current, $I_{OK}$ ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) . . . . . ±20 mA
Continuous output current, $I_O$ ($V_O = 0$ to $V_{CC}$) . . . . . ±35 mA
Continuous current through $V_{CC}$ or GND . . . . . ±70 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DW package . . . . . 97°C/W
N package . . . . . 67°C/W
Storage temperature range, $T_{stg}$ . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

## recommended operating conditions

| | | | SN54HCT373 | | | SN74HCT373 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | NOM | MAX | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | | 4.5 | 5 | 5.5 | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 4.5 V to 5.5 V | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 4.5 V to 5.5 V | 0 | | 0.8 | 0 | | 0.8 | V |
| $V_I$ | Input voltage | | 0 | | $V_{CC}$ | 0 | | $V_{CC}$ | V |
| $V_O$ | Output voltage | | 0 | | $V_{CC}$ | 0 | | $V_{CC}$ | V |
| $t_t$ | Input transition (rise and fall) time | | 0 | | 500 | 0 | | 500 | ns |
| $T_A$ | Operating free-air temperature | | –55 | | 125 | –40 | | 85 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | $V_{CC}$ | $T_A$ = 25°C | | | SN54HCT373 | | SN74HCT373 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $V_{OH}$ | $V_I = V_{IH}$ or $V_{IL}$ | $I_{OH}$ = –20 μA | 4.5 V | 4.4 | 4.499 | | 4.4 | | 4.4 | | V |
| | | $I_{OH}$ = –6 mA | | 3.98 | 4.3 | | 3.7 | | 3.84 | | |
| $V_{OL}$ | $V_I = V_{IH}$ or $V_{IL}$ | $I_{OL}$ = 20 μA | 4.5 V | | 0.001 | 0.1 | | 0.1 | | 0.1 | V |
| | | $I_{OL}$ = 6 mA | | | 0.17 | 0.26 | | 0.4 | | 0.33 | |
| $I_I$ | $V_I = V_{CC}$ or 0 | | 5.5 V | | | ±0.1 | ±100 | | ±1000 | | ±1000 | nA |
| $I_{OZ}$ | $V_O = V_{CC}$ or 0 | | 5.5 V | | | ±0.01 | ±0.5 | | ±10 | | ±5 | μA |
| $I_{CC}$ | $V_I = V_{CC}$ or 0, | $I_O$ = 0 | 5.5 V | | | 8 | | 160 | | 80 | μA |
| $\Delta I_{CC}$‡ | One input at 0.5 V or 2.4 V, Other inputs at 0 or $V_{CC}$ | | 5.5 V | | 1.4 | 2.4 | | 3 | | 2.9 | mA |
| $C_i$ | | | 4.5 V to 5.5 V | | 3 | 10 | | 10 | | 10 | pF |

‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or $V_{CC}$.

### timing requirements over recommended operating free-air temperature range (unless otherwise noted)

| | | $V_{CC}$ | $T_A$ = 25°C | | SN54HCT373 | | SN74HCT373 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_w$ | Pulse duration, LE high | 4.5 V | 20 | | 30 | | 25 | | ns |
| | | 5.5 V | 17 | | 27 | | 23 | | |
| $t_{su}$ | Setup time, data before LE↓ | 4.5 V | 10 | | 15 | | 13 | | ns |
| | | 5.5 V | 9 | | 14 | | 12 | | |
| $t_h$ | Hold time, data after LE↓ | 4.5 V | 10 | | 10 | | 10 | | ns |
| | | 5.5 V | 10 | | 10 | | 10 | | |

### switching characteristics over recommended operating free-air temperature range, $C_L$ = 50 pF (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ | $T_A$ = 25°C | | | SN54HCT373 | | SN74HCT373 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $t_{pd}$ | D | Q | 4.5 V | | 25 | 35 | | 53 | | 44 | ns |
| | | | 5.5 V | | 21 | 32 | | 48 | | 40 | |
| | LE | Any Q | 4.5 V | | 28 | 35 | | 53 | | 44 | |
| | | | 5.5 V | | 25 | 32 | | 48 | | 40 | |
| $t_{en}$ | $\overline{OE}$ | Any Q | 4.5 V | | 26 | 35 | | 53 | | 44 | ns |
| | | | 5.5 V | | 23 | 32 | | 48 | | 40 | |
| $t_{dis}$ | $\overline{OE}$ | Any Q | 4.5 V | | 23 | 35 | | 53 | | 44 | ns |
| | | | 5.5 V | | 22 | 32 | | 48 | | 40 | |
| $t_t$ | | Any Q | 4.5 V | | 10 | 12 | | 18 | | 15 | ns |
| | | | 5.5 V | | 9 | 11 | | 16 | | 14 | |

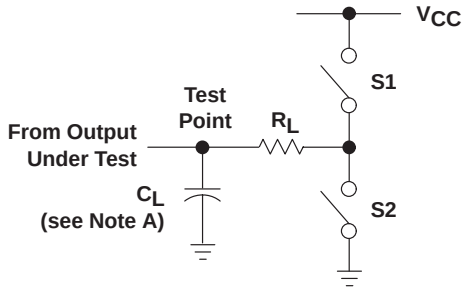
### switching characteristics over recommended operating free-air temperature range, $C_L$ = 150 pF (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ | $T_A$ = 25°C | | | SN54HCT373 | | SN74HCT373 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $t_{pd}$ | D | Q | 4.5 V | | 32 | 52 | | 79 | | 65 | ns |
| | | | 5.5 V | | 27 | 47 | | 71 | | 59 | |
| | LE | Any Q | 4.5 V | | 38 | 52 | | 79 | | 65 | |
| | | | 5.5 V | | 36 | 47 | | 71 | | 59 | |
| $t_{en}$ | $\overline{OE}$ | Any Q | 4.5 V | | 33 | 52 | | 79 | | 65 | ns |
| | | | 5.5 V | | 28 | 47 | | 71 | | 59 | |
| $t_t$ | | Any Q | 4.5 V | | 18 | 42 | | 63 | | 53 | ns |
| | | | 5.5 V | | 16 | 38 | | 57 | | 48 | |

### operating characteristics, $T_A$ = 25°C

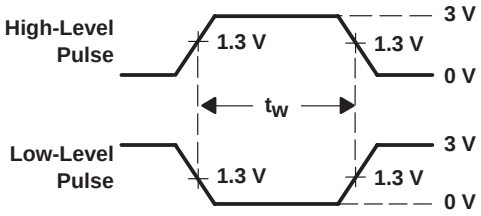
| PARAMETER | | TEST CONDITIONS | TYP | UNIT |
|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance per latch | No load | 50 | pF |

## PARAMETER MEASUREMENT INFORMATION

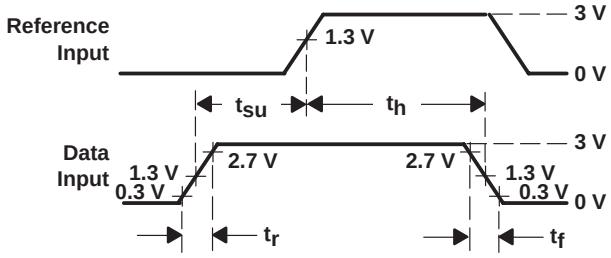



LOAD CIRCUIT

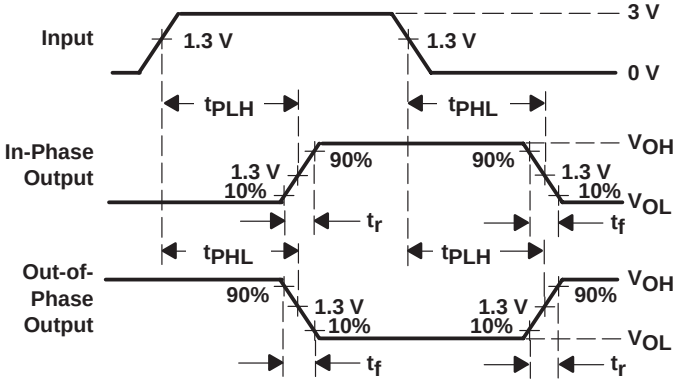
| PARAMETER | | $R_L$ | $C_L$ | S1 | S2 |
|---|---|---|---|---|---|
| $t_{en}$ | $t_{PZH}$ | 1 kΩ | 50 pF or 150 pF | Open | Closed |
| | $t_{PZL}$ | | | Closed | Open |
| $t_{dis}$ | $t_{PHZ}$ | 1 kΩ | 50 pF | Open | Closed |
| | $t_{PLZ}$ | | | Closed | Open |
| $t_{pd}$ or $t_t$ | | –– | 50 pF or 150 pF | Open | Open |



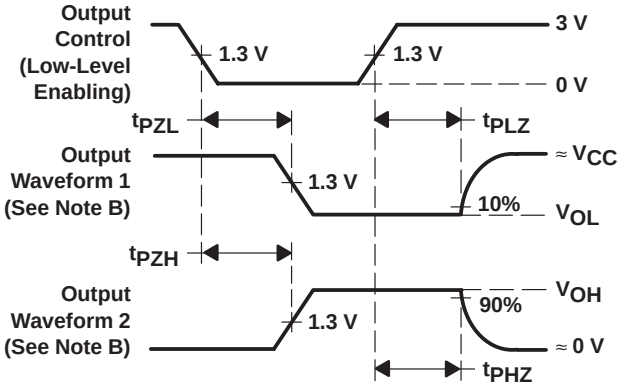

VOLTAGE WAVEFORMS
PULSE DURATIONS




VOLTAGE WAVEFORMS
SETUP AND HOLD AND INPUT RISE AND FALL TIMES




VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT RISE AND FALL TIMES




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES FOR 3-STATE OUTPUTS

NOTES: A. $C_L$ includes probe and test-fixture capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ = 6 ns, $t_f$ = 6 ns.
D. The outputs are measured one at a time with one input transition per measurement.
E. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
F. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.
G. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd}$.

**Figure 1. Load Circuit and Voltage Waveforms**

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